Docket No.: 20910/0205435-US0
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Michael D. Estlick et al.

Patent No.: 7,206,916

Issued: April 17, 2007

For: PARTIAL ADDRESS COMPARES STORED IN TRANSLATION LOOKASIDE BUFFER

REQUEST FOR CERTIFICATE OF CORRECTION PURSUANT TO 37 CFR 1.323

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected. A listing of the errors to be corrected is attached.

The typographical errors marked with an "A" on the attached list are found in the application as filed by applicant. Please charge our Credit Card in the amount of $100.00 covering the fee set forth in 37 CFR 1.20(a).

The errors now sought to be corrected are inadvertent typographical errors the correction of which does not involve new matter or require reexamination.

Transmitted herewith is a proposed Certificate of Correction effecting such corrections. Patentee respectfully solicits the granting of the requested Certificate of Correction.

The Commissioner is authorized to charge any deficiency of up to $300.00 or credit any excess in this fee to Deposit Account No. 04-0100.

Dated: May 7, 2007

Respectfully submitted,

By _____

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,206,916

APPLICATION NO.: 10/795,815

ISSUE DATE : April 17, 2007

INVENTOR(S) : Estlick, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 2, line 31, delete "information;" and insert - - information. - -, therefor.

In column 10, line 47, in Claim 15, delete "the" before "translation".

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Issued Patent Proofing Form
Note: **P** = PTO Error

A = Applicant Error

File#: **20910/0205435-US0**

US Serial No.: **10/795,815** US Patent No.: **US 7,206,916 B2** Issue Dt.: **Apr. 17, 2007**

Title: **PARTIAL ADDRESS COMPARES STORED IN TRANSLATION LOOKASIDE BUFFER**

Sr. No.	P/A	Original		Issued Patent		Description Of Error
		Page	Line	Column	Line	
1	A	Page 3 Specification (03/08/2004)	16	2	31 (Approx.)	Delete "information;" and insert - - information. - -, therefor.
2	A	Page 9 Claims (10/23/2006)	Claim 15 Line 8	10	47 (Approx.)	In Claim 15, delete "the" before "translation".

PARTIAL ADDRESS COMPARES STORED IN TRANSLATION LOOKASIDE BUFFER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of processors and more particularly to translation lookaside buffers within processors.

2. Description of the Related Art

In computer systems it is known for a processor to have a cache memory to speed up memory access operations to main memory of the computer system. The cache memory is smaller, but faster than main memory. It is placed operationally between the processor and main memory. During the execution of a software program, the cache memory stores more frequently used instructions and data. Whenever the processor needs to access information from main memory, the processor examines the cache first before accessing main memory. A cache miss occurs if the processor cannot find instructions or data in the cache memory and is required to access the slower main memory. Thus, the cache memory reduces the average memory access time of the processor.

In known computer systems, it is common to have a process executing only in main memory ("physical memory") while a programmer or user perceives a much larger memory which is allocated on an external disk ("virtual memory"). Virtual memory allows for very effective multi-programming and relieves the user of potential constraints associated with the main memory. To address the virtual memory, many processors contain a translator to translate virtual addresses in virtual memory to physical addresses in physical memory, and a translation lookaside buffer ("TLB"), which caches recently generated virtual-physical address pairs. The TLBs allow faster access to main memory by skipping the mapping process when the translation pairs already exist. A TLB entry is like a cache entry where a tag includes portions of the virtual address and a data portion includes a physical page frame number.

One aspect of processor performance relates to monitoring certain addresses such as instruction addresses via, for example, a watchpoint address or a sample address range. When monitoring the instruction address, it becomes important to quickly compare the instruction address against the watchpoint address or the sample address range. When a match is detected between the instruction address and the monitoring address, the processor takes some sort of action such as generating a watchpoint trap if the address matches the watchpoint address or collecting sampling information if the instruction address is within the sample address range.

SUMMARY OF THE INVENTION

In accordance with the present invention, a method for performing a fast information compare within a processor is set forth in which a more significant bit compare is performed when information is being loaded into a translation lookaside buffer. The result of the more significant bit compare is stored within the translation lookaside buffer as part of an entry containing the information. When the fast compare is desired, the result of the more significant bit compare is used in conjunction with results from a compare of less significant bits of the information and less significant bits of a compare address to determine whether a match is present.

In one embodiment, the invention relates to a method of performing a fast information compare within a processor which includes performing a more significant bit compare when information is loaded into a translation lookaside buffer, storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information, and using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present. The more significant bit compare compares more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information.

In another embodiment, the invention relates to an apparatus for performing a fast information compare within a processor which includes means for performing a more significant bit compare when information is loaded into a translation lookaside buffer, means for storing a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information, and means for using the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present. The more significant bit compare compares more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information.

In another embodiment, the invention relates to a processor which includes a translation lookaside buffer, a first compare unit coupled to the translation lookaside buffer and a second compare unit coupled to the translation lookaside buffer. The first compare unit performs a more significant bit compare when information is loaded into a translation lookaside buffer. The more significant bit compare compares more significant bits of the information being loaded into the translation lookaside buffer with more significant bits of compare information. The first compare unit stores a result of the more significant bit compare within the translation lookaside buffer as part of an entry containing the information. The second compare unit processor uses the result of the more significant bit compare in conjunction with results from a compare of less significant bits of the information and less significant bits of compare information to determine whether a match is present.

In another embodiment, the invention relates to a processor which includes a memory management unit and an instruction fetch unit. The memory management unit includes a memory management unit translation lookaside buffer. The instruction fetch unit includes an instruction translation lookaside buffer. The more significant bit compare is performed when information is loaded into the instruction translation lookaside buffer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference number throughout the several figures designates a like or similar element.

FIG. 1 shows a schematic block diagram of a processor architecture.

What is claimed is:

1. A method of performing a fast information compare within a processor comprising:

performing a first comparison when a first information is loaded into a translation lookaside buffer; comparing bits corresponding to a page number of the first information being loaded into the translation lookaside buffer with bits corresponding to a page number of a compare information;

storing a result of the first comparison within the translation lookaside buffer as part of an entry corresponding to the first information; and

using the stored result in conjunction with a second comparison comparing bits corresponding to a page offset of a second information and bits corresponding to a page offset of the compare information to determine whether a match is present between the second information and the compare information.

2. The method of claim 1 further comprising:

providing an indication of a match to the compare information when the stored result is active and the bits corresponding to a page offset of the second information match the bits corresponding to a page offset of the compare information.

3. The method of claim 1 wherein:

the compare information corresponds to a virtual address watchpoint.

4. The method of claim 1 wherein:

the compare information corresponds to a sample selection criteria.

5. The method of claim 4 wherein:

the sample selection criteria includes a first address and a second address corresponding to an address range; and

the result of the first comparison indicates whether the bits corresponding to a page number of the first information being loaded correspond to one of a plurality of conditions indicating whether a page corresponding to the first information is entirely inside the range, entirely outside the range, includes the entire range, includes the first address and includes the second address.

6. The method of claim 1 wherein:

the processor includes a memory management unit translation lookaside buffer and an instruction translation lookaside buffer; and

the first comparison is performed when the first information is loaded into the instruction translation lookaside buffer.

7. The method of claim 1 wherein:

the processor includes a plurality of threads; and

the compare information corresponds to one of the plurality of threads.

8. An apparatus for performing a fast information compare within a processor comprising:

means for performing a first comparison when a first information is loaded into a translation lookaside buffer, comparing bits corresponding to a page number of the first information being loaded into the translation lookaside buffer with bits corresponding to a page number of a compare information;

means for storing a result of the first comparison within the translation lookaside buffer as part of an entry corresponding to the first information; and

means for using the stored result in conjunction with a second comparison comparing bits corresponding to a page offset of a second information and bits corresponding to a page offset of the compare information to determine whether a match is present between the second information and the compare information.

9. The apparatus of claim 8 further comprising:

means for providing an indication of a match to the compare information when the stored result is active and the bits corresponding to a page offset of the second information match the bits corresponding to a page offset of the compare information.

10. The apparatus of claim 8 wherein:

the compare information corresponds to a virtual address watchpoint.

11. The apparatus of claim 8 wherein:

the compare information corresponds to a sample selection criteria.

12. The apparatus of claim 11 wherein:

the sample selection criteria includes a first address and a second address corresponding to an address range; and

the result of the first comparison indicates whether the bits corresponding to a page number of the first information being loaded correspond to one of a plurality of conditions indicating whether a page corresponding to the first information is entirely inside the range, entirely outside the range, includes the entire range, includes the first address and includes the second address.

13. The apparatus of claim 8 wherein:

the processor includes a memory management unit translation lookaside buffer and an instruction translation lookaside buffer; and

the first comparison is performed when the first information is loaded into the instruction translation lookaside buffer.

14. The apparatus of claim 8 wherein:

the processor includes a plurality of threads; and

the compare information corresponds to one of the plurality of threads.

15. A processor comprising:

a translation lookaside buffer; and

a first compare unit coupled to the translation lookaside buffer, the first compare unit performing a first comparison when a first information is loaded into a translation lookaside buffer, comparing bits corresponding to a page number of the first information being loaded into the translation lookaside buffer with bits corresponding to a page number of a compare information, the the translation lookaside buffer storing a result of the first comparison within the translation lookaside buffer as part of an entry corresponding to the first information; and

a second compare unit coupled to the translation lookaside buffer, the second compare unit using the stored result in conjunction with a second comparison comparing bits corresponding to a page offset of a second information and bits corresponding to a page offset bits of the compare information to determine whether a match is present between the second information and the compare information.

16. The processor of claim 15 wherein:

the second compare unit provides an indication of a match to the compare information when the stored result is active and the bits corresponding to a page offset of the second information match the bits corresponding to a page offset of the compare information.

17. The processor of claim 15 wherein:

the compare information corresponds to a virtual address watchpoint.